What is claimed is:

1. A pixel sensor for providing image sensing under radiation or space environment, comprising:

a readout circuit operating to convert optical image signals to electronic signals, where said readout circuit includes p-type transistors and an n-type photosensitive element; and

a first reset circuit configured to provide a reset level for a pixel output, where said first reset circuit includes at least one p-type transistor,

where said readout circuit and said first reset circuit having said p-type transistors, and said n-type photosensitive element, provide radiation hardness without any radiation protective enclosure.

2. The pixel sensor of claim 1, wherein said p-type transistors are MOSFET p-type transistors.

3. The pixel sensor of claim 1, wherein said n-type photosensitive element is an n-type photodiode.

4. The pixel sensor of claim 3, wherein said n-type photodiode is formed in a square layout design.

5. The pixel sensor of claim 3, wherein said n-type photodiode is formed in a circular layout design.

6. The pixel sensor of claim 1, further comprising:

a p-type substrate on which said n-type photosensitive element is formed.

7. The pixel sensor of claim 6, further comprising:

a pair of p+ type guard rings formed on said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings connected to a ground voltage, and operating to substantially reduce a leakage current from said n-type photosensitive element.

8. The pixel sensor of claim 6, further comprising:

an n-type well provided adjacent to said p-type substrate, said n-type well connected to a supply voltage, and operating to prevent crosstalk between pixels.

9. The pixel sensor of claim 1, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

10. A radiation-hard CMOS image sensing device, comprising:

a p-type substrate;

an n-type photodiode formed on said p-type substrate, where said n-type photodiode operates to convert an optical signal to an electrical signal;

a first reset circuit configured to provide a reset value for said electrical signal, said first reset circuit including a p-type MOSFET transistor; and

a readout circuit operating to buffer said electrical signal, said readout circuit including a p-type MOSFET transistor.

11. The device of claim 10, further comprising:

a pair of p+ type guard rings formed on said p-type substrate, each of said pair of guard rings formed on either side of said n-type photodiode, said pair of guard rings connected to a ground voltage, and operating to substantially reduce a leakage current from said n-type photodiode.

12. The device of claim 11, further comprising:

an n-type well provided adjacent to said p-type substrate, said n-type well connected to a supply voltage, and operating to prevent crosstalk between pixels in the CMOS image sensing device.

13. The device of claim 10, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

14. A CMOS image sensor system, comprising:

an array of active pixel sensors, each pixel sensor of said array including:

a pixel readout circuit operating to convert optical image signals to electronic signals, where said pixel readout circuit includes p-type transistors and an n-type photosensitive element, and

a first reset circuit configured to provide a reset level for a pixel output, where said first reset circuit includes p-type transistors,

where said pixel readout circuit and said first reset circuit having said p-type transistors and said n-type photosensitive element provide radiation hardness without any radiation protective enclosure;

a control circuit configured to provide timing and control signals to enable read out of data stored in said array of active pixel sensors; and

a column readout circuit operating to receive and process said data stored in said array of active pixel sensors.

15. The CMOS image sensor of claim 14, further comprising:

a p-type substrate on which said n-type photosensitive element is formed.

16. The CMOS image sensor of claim 15, further comprising:

a pair of p+ type guard rings formed on said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings connected to a ground voltage, and operating to substantially reduce a leakage current from said n-type photosensitive element.

17. The CMOS image sensor of claim 15, further comprising:

an n-type well provided adjacent to said p-type substrate, said n-type well connected to a supply voltage, and operating to prevent crosstalk between pixels.

18. The CMOS image sensor of claim 14, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.